REMARKS

I. Introduction

Claims 1 to 8 are currently pending in the present application. Claims 1 and 5 have been amended. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration of the present application is respectfully requested.

II. Rejection of Claims 1 to 8 Under 35 U.S.C. § 103(a)

Claims 1 to 8 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,567,335 ("Norman et al."). Applicants respectfully submit that Norman et al. do not render unpatentable the present claims for the following reasons.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish *prima facie* obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). It is respectfully submitted that Norman et al. do not disclose or suggest all of the features recited in independent claim 1 or independent claim 5.

Claim 1 recites, *inter alia*, a memory arrangement that includes a first buffer memory and a second buffer memory. Claim 1 recites that in the case of a command access, at least one command following an access command is written to the first buffer memory, and that in the case of a data access, at least one datum following accessed datum is written to the second buffer memory.

Norman et al. do not disclose, or even suggest, that: (1) in the case of a command access, at least one command following an access command is written to a first buffer memory; and (2) in the case of a data access, at least one datum following accessed datum is written to a second buffer memory. With respect to the command access, while the sections of Norman referenced in the Final Office Action may discuss an input buffer (48) to which is connected a Tag Bus (40) via which a Controller (36) may transfer control information, nowhere do Norman et al. disclose, or even suggest, that, for example, during a command access to receive in the input buffer (48) a command, at least one following

command is written to the input buffer (48). With respect to the data access, while the sections of Norman referenced in the Final Office action may discuss a buffer (52) to which data from Memory Devices (38) are written in accordance with the presence of a Tag written to the input buffer (48), nowhere do Norman et al. disclose, or even suggest, that, for example, during a data access by the Controller (36) via a Tag to receive data from the Memory Devices (38), at least one following datum is written to the buffer (52).

With respect to the independence of the writing of the at least one command following the accessed command and the writing of the at least one datum following the accesses datum, the "Response to Arguments" section of the Final Office Action asserts that this feature is disclosed by Norman et al. In this connection, the Examiner interprets the independence of the writing to mean that writing of one of the at least one command and the at least one datum does not require writing of the other at the same time. In order to clarify the claimed subject matter, claim 1 has been amended to recite "wherein the at least one command following the accessed command and the at least one datum following the accessed datum are written irrespective of their association with one another."

Norman et al. do not disclose, or even suggest, writing at least one command following an accessed command and at least one datum following an accessed datum irrespective of their association with one another. Norman et al. indicate that when a special Tag is present on a Tag bus (40), a respective output on a data bus (42) is generated. Thus, the "commands" on bus (40) directly control the data flow as to address mapping and memory control, and thus are not written irrespective of their association with one another. For instance, on col. 6, lines 15-22, it is stated that when a Tag (19h) is present on the Tag bus (40), data is read out of the device, and when a Tag (1a) is on the Tag bus (40), the contents of a control register are read out of the device. Thus, these commands control data flow. Furthermore, the input enable IEN, which connects buffers (48) and (52), shows that the buffers are not independent of each other. Taken as a whole, in contrast to the claimed subject matter, Norman et al. disclose a conventional memory control strategy in which, if there is a jump command, associated data is written, so that the writing of data is not irrespective of its association with the command. In particular, if a special Tag is provided, a corresponding reaction in buffer (52) is established.

The claimed arrangement provides certain advantages over the conventional strategy in that there is no wait time needed between commands and corresponding data, or vice versa, because they are written independently of each other and stored automatically irrespective of their association with one another. Thus, the claimed arrangement provides a time saving and an increase of memory performance which is not disclosed or suggested by Norman et al., since the arrangement of Norman relies on a dependence between the two

buffers. See also, Norman et al., col. 6, lines 47 to 51 (indicating that data received on bus (42) is also used in conjunction with various commands present on the Tag bus (40) for performing various memory control functions).

For at least these reasons, it is respectfully submitted that Norman et al. do not render unpatentable claim 1, or claims 2 to 4, which depend from claim 1.

Claim 5 relates to a method for performing at least one of command access and data access during a program execution in connection with a programmable memory. Claim 5 recites that the method includes the steps of: recognizing in the case of a command access that a command access is present; recognizing in the case of a data access that a data access is present; writing a command following the accessed command to a first buffer memory; and writing a datum following the accessed datum to a second buffer memory; and that the command and the datum are written in the writing steps irrespective of their association with one another.

As more fully set forth above with respect to claim 1, it is respectfully submitted that Norman et al. do not disclose, or even suggest, writing a command following an accessed command, or writing a datum following an accessed datum, let alone that they are written irrespective of their association with one another.

For at least these reasons, it is respectfully submitted that Norman et al. do not render unpatentable claim 5, or claims 6 to 8, which ultimately depend from claim 5.

In view of the foregoing, withdrawal of this rejection is respectfully requested.

III. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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